

A Soft-Switched Voltage Source Inverter Topology

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Abstract—Soft-switching is a highly effective technique that enhances the efficiency and power density of power electronic converters. To achieve soft-switching in an inverter, a new approach involves the addition of two additional DC-link switches to the existing voltage source inverter setup. This research paper introduces the idea of achieving soft switching for the entire inverter using only a single hard switch. The study includes a comprehensive analysis of the proposed topology, encompassing loss calculations and parameter design, particularly focusing on steady-state conditions. To validate the proposed concept, a 1 kW single-phase inverter model is simulated using MATLAB/Simulink. The results indicate that the proposed topology outperforms the conventional H-Bridge configuration in terms of efficiency.

Index Terms—VSI Topology, Zero voltage switching(ZVS), Soft-switching.

I. INTRODUCTION

The dominance of voltage source inverters in power generation, motor drives, and other applications stems from their versatility [1]. There is a prevailing tendency in the industry to enhance the power density of converters, resulting in cost savings through reduced physical material and fewer components in the development of commercial inverters [2].

To improve the power density of the converter, it is advisable to operate the inverter at a higher switching frequency, which leads to a reduction in reactive filter requirement of the converter [3]. Increasing the switching frequency produces higher switching losses, reducing converter efficiency. Commercial MOSFET-based inverters typically have a maximum switching frequency of 20 kHz [4].

To overcome this challenge in developing high-frequency inverters, soft-switching methods can be utilized to increase the converter's power density while obtaining high efficiencies. There has been extensive research in the literature on achieving soft switching for inverter switches using the ZVS or ZCS condition [5], [6]. Most of them can be divided into two parts: resonant DC-link and resonant AC-link.

In the year 1989, Divan [7] introduced the concept of a resonant DC-link (RDCL) soft-switching inverter. A resonant circuit in the DC-link is a commonly employed technique in inverters. By achieving resonance in the circuit, it is possible to observe instances where the voltage is reduced to zero. By switching the inverter switches during these specific moments

it is possible to mitigate power losses; however, it also presents a drawback of high voltage stress and integral pulse density modulation is used to achieve soft switching. A review paper on the resonant DC-link inverter [13] concludes that these types of circuits are not suitable for PWM techniques due to their lack of a function that allows for a continuous variation of the pulse width. To tackle this challenge, some modification of the Resonant DC-link inverter is present: active clamped resonant DC-link and quasi-resonant DC-link inverter [8] - [10].

Quasi-resonant soft-switching technique works on the traditional PWM techniques. In these inverters, the input power supply is separated from the inverter DC-link by a switch, called DC-link switch. Also, a resonant capacitor is placed in parallel with the inverter DC-link. When a change in the state of inverter switches is necessary, the DC-link switch is turned off, and the resonant capacitor discharges by an auxiliary circuit, and thus, the state of inverter switches can be changed under ZVS condition [12] and [17].

The main objective of quasi-resonant DC-link inverters is to attain soft switching conditions with minimal reliance on auxiliary circuit components. The auxiliary circuit comprises two or three auxiliary switches. By reducing the number of auxiliary switches, the control circuit becomes simpler and the overall cost of the inverter decreases. Therefore, it is recommended to explore the possibility of developing soft-switching inverters with just a minimum number of auxiliary switches [13] - [15].

In Load-side ZVS, an auxiliary circuit produces a transition period to bring ZVS through a resonance, which is shorter than the switching cycle. The resonance usually happens between the resonant inductors and the parasitic capacitors of the inverter's switches with the assistance of additional auxiliary switches.

In [15] an auxiliary resonant commuted pole adds three half-bridges with a series resonant inductor to the load terminal. During the transition period, it will create resonance between resonant inductors and the output capacitors of the inverter's switches and its facilitate zero voltage transition (ZVT) to the inverter's switches. However, it requires a larger number of components, so it is suitable for large three-phase power applications. A few different types of load-side soft switching are proposed in [14] and [15].

The author conducts an extensive investigation of soft-switching techniques. The author encountered various challenges:

- Not all soft-switching topologies are universal, so finding the right soft-switching for your specific applications can be challenging.
- The ability of soft switching to achieve ZVS depends on the power factor of the load. Some techniques may only achieve ZVS for a specific range of power factors.
- Achieving soft-switching may not always be possible with the absolute minimum number of auxiliary components.
- The ability of a soft-switching technique to achieve ZVS across a wide load range varies. Some techniques may have a limited ZVS range.

To address the limitations of complex control and bulky auxiliary components in existing VSI designs, the author proposes a novel generalized topology that significantly reduces component count while maintaining high efficiency and ZVS capabilities.

The rest of paper is organize as follow Analysis of the proposed topology is present in section II, parameter design inverter is present in section III. while section IV focuses on the simulation and result validation.

II. ANALYSIS OF PROPOSED TOPOLOGY

To showcase the functionality of the proposed topology, a two-level single-phase VSI is used as a demonstration platform. The key element of the proposed topology is an auxiliary circuit strategically placed between the DC-link and the VSI input, as highlighted in fig.1 The highlighted area consists of two auxiliary switches, referred to as S_A and S_B , respectively, and it facilitates the soft switching of the inverter.

The turn-off process is initiated by deactivating switch S_A . This action enables the load current to pass through the auxiliary path formed by activating switch S_B . The flow of this current, combined with the conduction of the body diode, facilitates zero voltage switching (ZVS) for switches S_1 and S_2 thereby resulting in a further reduction of losses.

The process of commutation exclusively employs active switches, thereby eliminating the requirement for bulky and sensitive passive components such as inductors and capacitors. This characteristic endows it with inherent versatility and resilience, ensuring effective operation irrespective of load fluctuations or types.

A. operation of proposed converter

The following assumption are considered to understand operating principle of the proposed converter.

- All active and passive devices that are considered ideal, including a DC source, switches, and capacitors, are equipped with internal switch diodes and capacitance.
- All switches are considered to be ideal, with zero resistance in the on state.
- The effects of parasitic capacitors on the inverter's switches are neglected.

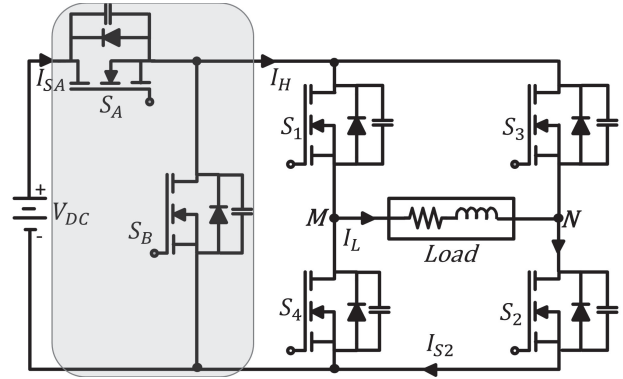


Fig. 1. Proposed topology

- Load inductor resistance is very low, so it is neglected.
- The residual store energy load is zero.
- Current always takes low resistance path.

The steady-state operating principle of the proposed topology is categorized into five modes, namely modes I to V, as illustrated in fig.2. Correspondingly, the operating wave-forms can be observed in fig.3.

1) *Mode 1* - ($t_0 \leq t_1$): This mode begins when S_A is turned on with a zero current condition. The load voltage is set to $+V_{DC}$, and the load current steadily rises from zero to its maximum value, depending on the load. This mode is also known as “active mode.” Fig.2(a) depicts an arrowhead indicating the direction of the current. The instantaneous voltage and current characteristics of the switches are described as follows:

$$V_{MN} = +V_{DC}, V_{SW1} = V_{SW2} = V_{SA} = 0, \\ V_{SW3} = V_{SW4} = +V_{DC}, I_{Sw1} = I_{Sw2} = I_{SA} = I_H = I_L.$$

2) *Mode 2* - ($t_1 \leq t_2$): After time instant t_1 , the DC-link switch S_A is turn-off under hard switching. The load current is trying to complete its path via the diode D_{SB} . Fig.2(c) depicts the flow direction of the current. The voltage potential across points M and N is zero. The instantaneous voltage and current characteristics of the switches are described as follows:

$$V_{MN} = 0, V_{SW1} = V_{SW2} = V_{SB} = 0, \\ I_{Sw1} = I_{Sw2} = I_H = D_{SB} = I_L.$$

3) *Mode 3* - ($t_2 \leq t_3$): Prior to instant t_2 , the diode D_{SB} begins conduction, causing the switch S_B to be triggered in the ZVS. Now, the load current is trying to complete its path through the switch S_{SB} . Fig.2(d) illustrates the flow direction of the current. At instant t_5 , the voltage across switch V_{SW1} and V_{SW2} is equivalent to the voltage drop across switch S_B , which is ideally zero and practically one or two volts. Consequently, at this voltage level, both switch S_1 and switch S_2 are turns-off. The voltage potential across points M and N is zero. The instantaneous voltage and current characteristics of the switches are described as follows:

$$V_{MN} = 0, V_{SW1} = V_{SW2} = V_{SB} = 0, \\ I_{Sw1} = I_{Sw2} = I_{SB} = I_H = D_{SB} = 0.$$

4) *Mode 4* - ($t_3 \leq t_4$): After time instant t_3 , the inverter switch S_1 and S_2 turn-off. The load current is trying to complete its path via the diode D_{S3} and D_{S4} . Fig.2(d) depicts

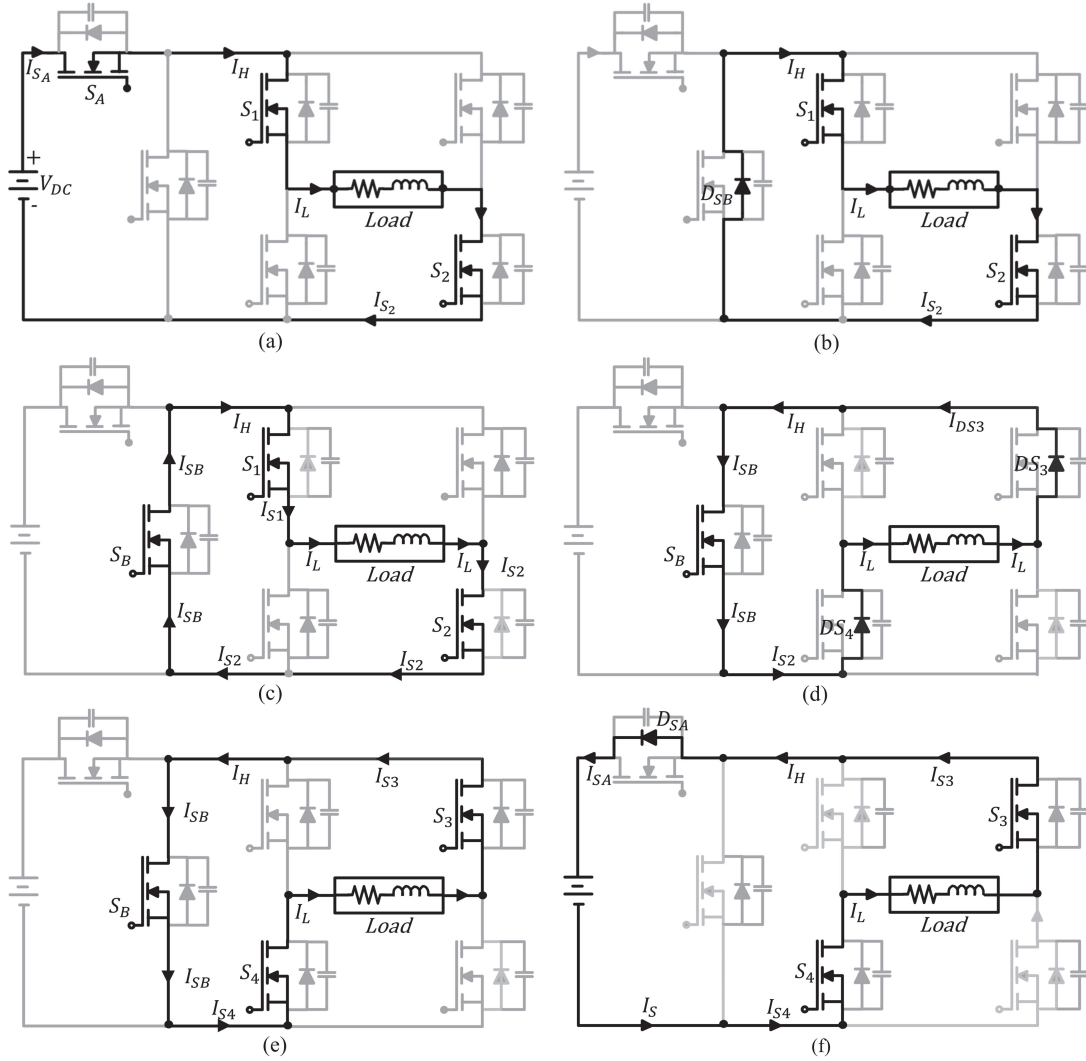


Fig. 2. operating modes of proposed topology

the flow direction of the current. The voltage potential across points M and N is zero. The instantaneous voltage and current characteristics of the switches are described as follows:

$$V_{MN} = 0, V_{SW1} = V_{SW2} = V_{SB} = 0, \\ I_{SB} = I_{DS4} = I_{DS3} = I_{SB} = I_H = I_L.$$

5) *Mode 5* - ($t_4 \leq t_5$): Before instant t_4 , the diodes D_{S3} and D_{S4} commence conduction, causing the switches S_3 and S_4 to be turned on in the ZVS. Now free-wheel current tries to complete its path through the switch S_{SB} . Fig.2(e) illustrates the flow direction of the current and switch S_B . At the end of this mode, instantaneous voltage and current of the switches are as follow:

$$V_{MN} = 0, V_{SW3} = V_{SW4} = 0, V_{SA} = V_{DC}, \\ I_{Sw3} = I_{Sw4} = I_{SB} = I_H = I_L.$$

6) *Mode 6* - ($t_5 \leq t_6$): After instant t_6 , if the free-wheeling current is not zero, the switch S_B will be turned off under hard-switching. In this scenario, the free-wheeling current

attempts to find its path through the diode D_{SA} . Fig.2(f) illustrates the flow direction of the current. At the end of this mode, the instantaneous voltage and current of the switches are as follows:

$$V_{MN} = 0, V_{SW1} = V_{SW2} = \frac{V_{DC}}{2}, V_{SB} = V_{DC}, \\ V_{SA} = 0, I_{Sw3} = I_{Sw4} = I_H = I_L.$$

III. PARAMETER DESIGN

In this section the design aspects of the single-phase VSI are described, furthermore a discussion and explanation about different decisions adopted is faced up. The optimum designing of the inverter is mainly depends upon the various factors like Voltage, Current, Power and Modulation scheme are adopted for the efficient inverter design. The design of the filter in this proposed topology is contingent upon the specific application of the VSI. Since the application can vary, the design of the filter is not fixed and therefore not included in this section.

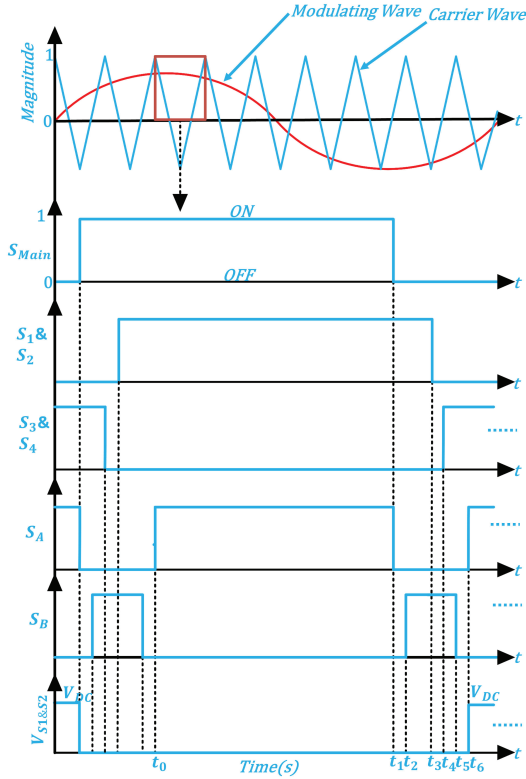


Fig. 3. Operating Waveform

A. DC Link Bus Capacitor

In a single-phase two-level VSI, the input capacitor is used for following purpose [20].

- To reduce the spread of current harmonics into the DC source.
- To supply the input pulsed current of the inverter.
- To supply power during transient-peak and to protect inverter from the transient peak of the DC-link voltage.

The calculation of the minimum capacitance value required on the DC bus can be determined using the equations provided in [20]. The author specified output power $P_{out} = 1kW$, DC_{bus} voltage = 200V, and output frequency $F_{out} = 60Hz$.

$$C_{Bus} = \frac{4 \times P_{out} \times t_1}{V_{BUS}^2} = \frac{4 \times 1000 \times 0.00416}{200^2} = 416\mu F \quad (1)$$

Where as t_1 is given by:

$$t_1 = \frac{1}{4 \times F_{OUT}} = \frac{1}{4 \times 60} = 0.0416s \quad (2)$$

The inverter implementation requires a selected total capacitance that is approximately double the calculated value. This capacitance should be rated at 500V and have an Maximum

operating temperature of $105^\circ C$. As per calculations and guidelines bus capacitor $832\mu F$ is selected for the simulation validation.

B. Switch Selection

1) *Transient Model*: In the active state, a load current begins to flow, and the transient model can be utilized to determine the instantaneous current. The development of the transient model is based on the following assumptions:

- All switches are assumed to be ideal on state resistance of the switch is zero.
- The voltage drop across the parasitic capacitor is extremely minimal, thus it can be disregarded.
- During the active state body diode is reverse biased so it is neglected.
- Step response is applied to the circuit fig.2(a)
- In the analysis of R-L load, the chosen topology remains unaffected by load variations.

Apply KVL in the fig.2(a).

$$L \frac{di_l}{dt} + Ri(t) = V_{DC} \quad (3)$$

In (3), it is a first-order differential equation and assumes that the current value reaches its peak value at the T/2 period. The solution of the above equation is given by:

$$\frac{V_{DC} \left[1 + e^{-\frac{T}{2\tau}} - 2e^{-\frac{T}{\tau}} \right]}{2 \left[1 + e^{-\frac{T}{2\tau}} \right]} = i(t) \quad (4)$$

It can be observed from (4), that the load current during the end of the positive half cycle is expected to be $-i_0$, as indicated by the symmetry of the load voltage.

$$i(t) = - \frac{V_{DC} \left[1 + e^{-\frac{T}{2\tau}} - 2e^{-\frac{(T-T)}{\tau}} \right]}{2 \left[1 + e^{-\frac{T}{2\tau}} \right]} \quad (5)$$

$$\tau = - \frac{L}{R} \quad (6)$$

Switches in each leg of the inverter operate in a complimentary manner. When upper switch of a leg is on the lower switch will need to block the entire DC bus voltage and vice versa. Thus, the switches must be rated to block the worst-case instantaneous magnitude of DC voltage.

In practical VSI, the voltage rating of the switching devices must exceed the worst-case DC bus voltage. This necessity arises from several factors, including:

- During turn-on, the switching device exhibits a momentary voltage spike exceeding the steady-state DC bus voltage. This transient may be caused by the stray inductance and stray capacitance.
- Switching events can generate momentary current surges due to the rapid change in device conductance. Overrating the switch current rating ensures it can handle these transient peaks without risk of failure.

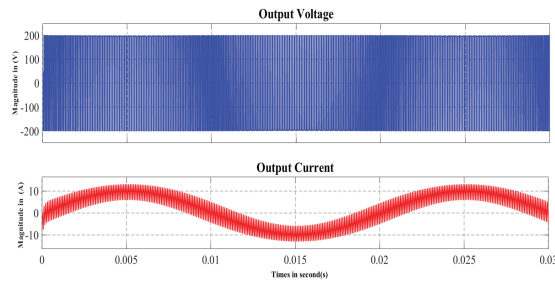


Fig. 4. Output Voltage and Current

For a well laid out circuit a 2.5 times DC bus voltage margin may be the optimum value for the conventional H-Bridge Inverter topology [18].

In accordance with our specifications, the maximum DC-link voltage for a conventional H-Bridge inverter is established at 200V and root mean square(RMS) value of the output current is 9.09A. To ensure a safety margin of 2.5 times the DC-link voltage, a device with a rating of 500V is chosen for the conventional inverter topology.

In this case, the IRFP460 has been selected based on its availability in the lab. All losses associated with this device are accounted for in the conventional H-Bridge inverter.

As proposed topology will provide the ZVS during turn on and turn-off period voltage and current transient can nullify so it will help us to select device at rated value. In our specification and requirement IR640N is selected. Auxiliary circuit switch S_A is only hard-switch so only one highly efficient device is required STW40N60M2-4.

IV. SIMULATION AND RESULT

The validation of the proposed converter topology working principle is carried out through the modeling and simulation. The simulation of the proposed topology is performed using principal components in MATLAB/Simulink, as shown in fig.1, and table I.

In this simulation, an ideal DC source is connected in series with a wire resistor $n\Omega$ and a wire inductor nH . MOSFET switches from the Specialize Power System Library are utilized to simulate the H-bridge section of the DC-AC inverter, which has a resistance of $0.27\text{ m}\Omega$ and a capacitance of 350 pF as a snubber.

In order to verify the functionality of the topology inverter running at a modulation index of 0.8 and a switching frequency of 10kHz, a load resistor and an inductor of 10Ω and 1mH respectively, are connected in the load side. The simulations employ a Bipolar (PWM) technique. Fig.4 depicts the voltage and current output of the inverter.

Figure illustrates the ZVS turn-on of MOSFET switch, with the current following a specific pattern. It rises when the gate pulse is triggered and returns to zero just before the gate pulse reaches zero. This mechanism enables the achievement

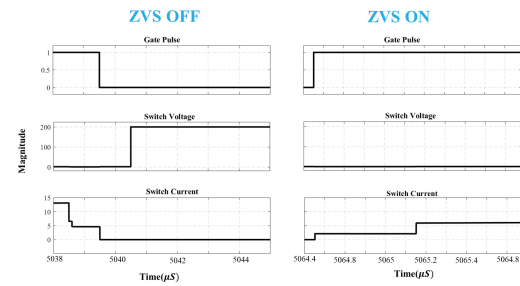


Fig. 5. Soft switching validation of proposed topology

TABLE I
SIMULATION PARAMETERS

Parameters	Values
Rated Power	1kW
DC link voltage	200V
DC link capacitor	$832\mu\text{F}$
Switching frequency	10kHz
MOSFET for the conventional H-Bridge Inverter	IRFP460
MOSFET for the Proposed Inverter	IR640N
MOSFET used in auxiliary circuit	STW40N60M2
Switch on state resistance	0.27Ω
Body diode forward voltage drop	0.5V
Body diode on state resistance	$80\text{m}\Omega$
Load resistor	10Ω
Load inductor	1mH

of ZVS. Consequently, these switches S_1 to S_4 are controlled by this ZVS, making it the suggested converter that maintains ZCZVS switching throughout the cycle.

Figure 6 illustrates the power losses of the switching devices in the proposed topology and conventional H-Bridge topology, both in active and zero modes. It is evident from fig. 6, that the proposed topology exhibits lower conduction loss and lower switching loss compared to the conventional H-Bridge inverter. This can be attributed to the introduction of a new two new DC-link switch.

On the loss calculations, it is found that the H-Bridge topology has a total of 52.88W and 79.11W of conduction and switching losses, respectively. For the proposed topology, it is found that it has a total of 28.01W and 16.01W of conduction and switching losses, respectively. Note that loss in the auxiliary circuit is included in the proposed topology.

A. Efficiency Evaluation

While the single-phase soft-switching inverter boasts reduced switching losses in its four main switches thanks to an auxiliary circuit, this addition also introduces auxiliary circuit

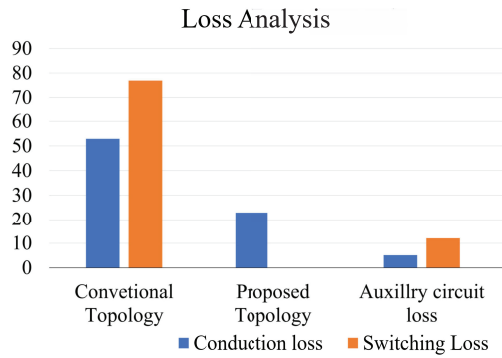


Fig. 6. power loss comparison

losses. However, if these auxiliary losses are outweighed by the reduction in main switch losses, the soft-switching inverter shines with improved efficiency over its hard-switching counterpart. The specific equation provided calculates the inverter efficiency of this proposed topology, allowing for evaluation of its performance compared to traditional designs.

$$\eta = \frac{P_{out}}{P_{out} + P_{conduction} + P_{auxiliary} + P_{switching}} \quad (7)$$

where,

$P_{conduction}$ = Conduction loss of the Inverter.

$P_{auxiliary}$ = Losses in auxiliary circuit.

$P_{switching}$ = Switching loss of the inverter.

The calculation reveals that the conventional H-Bridge inverter exhibits an efficiency of 88.62% for the given simulation parameter and at rated load. On the other hand, the proposed topology demonstrates an efficiency of approximately 95.25% at rated load.

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CONCLUSION

This paper proposes a novel full-range soft-switching voltage source inverter (VSI) employing a minimal two-switch auxiliary circuit. This distinct approach facilitates zero-current switching (ZCS) and zero-voltage switching (ZVS) operation, respectively, minimizing switching losses and achieving near-zero voltage-zero current switching (ZVZCS) with reduced control complexity. The proposed pulse-width modulation (PWM) techniques guarantee soft-switching across the entire operating range, leading to unprecedented full-range soft-switching capability.

Compared to conventional hard-switch inverters, the offered solution exhibits significantly reduced ripple in both input and output voltage and current. This allows for the utilization of the rated values for DC-link capacitors and switches, maximizing component efficiency and lifespan. Simulations validate the

theoretical analysis, showcasing a remarkable 6.63% increase in efficiency for a 1kW, 10kHz VSI operation, demonstrating the significant performance advantages of the proposed soft-switching VSI topology.

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